X-716-66-554

NASA TM X- 55758

A LOW NOISE SWITCHING CONVERTER-REGULATOR FOR MAIN POWER CONTROL IN A SPACE POWER SYSTEM

BY

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NOVEMBER 1966

GODDARD SPACE FLIGHT CENTER

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ABSTRACT

This report describes a variable ratio dc transformer regulator used in a voltage boost configuration to process the main vehicle power from a solar array battery power system in the Radio Astronomy Explorer (RAE) spacecraft. The selection of the design approach for the switching regulator is presented, together with an analysis of its operation and definition of its characteristics, functional performance, and test results.

The regulator transforms a variable voltage input to a constant average voltage by constant-frequency pulse width modulation. Two major advantages are high efficiency and essentially constant thermal dissipation over a wide range of input power. The boost configuration employs a power transformer and transistor switches to handle only boost power. This method significantly reduces the RF interference generated in switching as compared to other series-switching regulation techniques, for voltage set-up, or step-down.

The RF interference (RFI) inherent in the use of a switching regulator presented a major problem. The circuit elements, mode of regulation, and packaging arrangement were all developed to minimize RFI with the least sacrifice of performance.

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INTRODUCTION

The primary purpose of the Radio Astronomy Explorer (RAE) satellite project is to investigate long-wavelength emissions from the sun, the planets, and galactic and extragalactic sources. This satellite is designed to measure the intensity of radio signals from celestial sources as a function of frequency, direction, and time. It is intended to provide the first map of the galaxy at frequencies below ionospheric cutoff. Observations will be made in the frequency band from 0.2 MHz to 10 MHz.

With these objectives, it was mandatory that all flight equipment be designed with the best engineering practice to prevent interference within the specified frequency range. No transmission of signals having any measurable energy in this range could be tolerated, since such RF transmissions would be picked up by the receivers and mask the observational data. The sensitivity of the receivers ranges from -110 to -126 dbm.

One major source of RF interference (RFI) is from static power supplies which utilize switching techniques for voltage regulation. However, the use of switching regulators is otherwise advantageous, since they offer a significant efficiency and weight advantage as compared to conventional regulators. Suppression of electromagnetic interference within this type of power supply is inherently a trade-off of cleanliness for performance, since the design requirements of one generally conflict with the other.

Part I of this report defines the system aspects and requirements of the main bus regulator. Part II discusses the RFI considerations of the design, and the various approaches considered, along with the selection of the regulation technique. Part III presents a detailed analysis, along with performance characteristics, of the main bus regulator circuit.

PART I

POWER SYSTEM ASPECTS WITH THE MAIN BUS REGULATOR REQUIREMENTS

The position of the main bus regulator in the satellite's electric power and distribution subsystem is shown in figure 1.

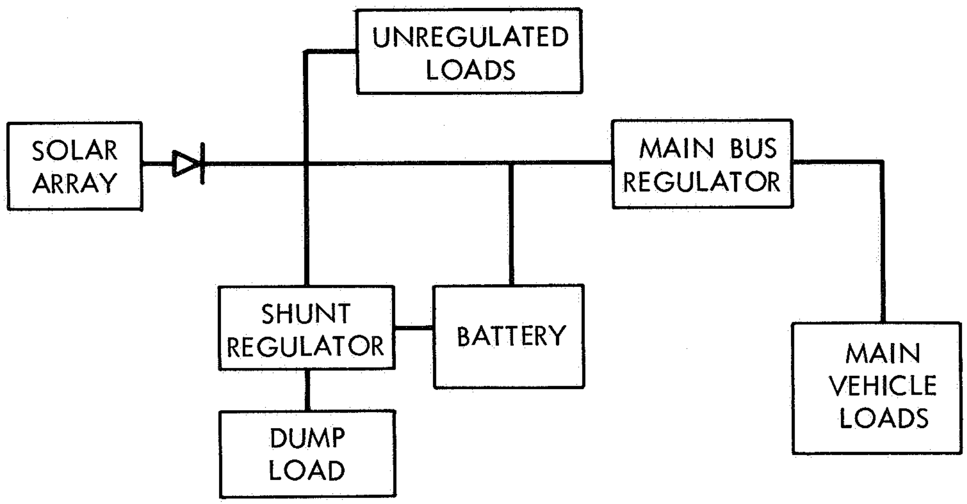


Figure 1–Simplified block diagram of electric power and distribution subsystem.

The solar array, which primarily supplies power for the vehicle loads, must also provide power to charge the vehicle battery. The major portion of the array power is passed directly to the input of the main bus regulator, while a smaller portion, appropriately controlled by the shunt regulator, is provided for charging the battery. A load is provided with the shunt regulator to act as a dump for excess solar power. The operating point on the solar array volt-ampere characteristic is established by the battery voltage. This voltage varies with the available solar power due to sun aspect and load requirements, thus producing a range of input voltage to the main bus regulator.

The main bus regulator must process the solar-array-battery power with this varying input voltage characteristic and provide a constant output voltage for all changing load conditions. A voltage step-up or boost regulator was chosen to accomplish this function.

The significant requirements imposed on this regulator were the following:

A. Electrical

1. RFI

a. Conducted – less than 1 microvolt (broadband and cw) from 0.15 to 10 MHz measured in accordance with Mil I 6181D.

b. Radiated – same as above but measured in accordance with Mil I 6181D at 3 inches from the unit.

2. Input 12-17 volts

a. Voltage ripple: less than 20 millivolts peak to peak.

3. Output 18 volts

a. Static Regulation: ±2%

<u>Range of Conditions</u>

(1) Input voltage: 12 to 17 volts from solar array or NiCd battery.

(2) Power output range: 4.5 to 45 watts.

(3) Temperature: -20°C to 50°C.

b. Dynamic regulation:

Condition	Maximum Voltage Over-shoot	Maximum Voltage Under-shoot	Maximum Response Time
(1) Input voltage: 12-17 volts step wave with $t_{rise} = t_{fall} < 3$ ms	10%	10%	1 ms
(2) Load current: 1.0 to 2.0 amperes step wave with $t_{rise} = t_{fall} < 10$ us	20%	20%	1 ms

c. Voltage ripple – less than 200 millivolts peak to peak.

B. Mechanical

Configuration: 2 main bus regulators in 1 package
Weight: less than 5 lbs.
Size: 5" × 7" × 3-1/4".

PART II

PRIMARY DESIGN CONSIDERATIONS

The dc to dc power conversion is accomplished in a static power supply by semiconductor switches turning on and off large blocks of current many times each second. The RFI generated by this switching is thus an important factor in the design of a semiconductor power supply. Ideally, perfect switches operating from a source of zero reactance would have zero commutation time; the current waveform through each switch would be a square wave; and the basic rectangular current wave reflected on the source would be a train of square pulses with zero dwell time between pulses, that is, pure dc. However, actual current pulses consist of a train of short, high amplitude, irregular waveforms of definite duration and repetition rate. This is broad band RFI, as contrasted to narrow band cw voltages or currents of sinusoidal shape. Depending on the configuration of the current-carrying path, certain portions of the frequency spectrum may radiate and set up electromagnetic waves in the surrounding regions. This constitutes radiated interference.

Every electrical circuit carrying time-varying voltages or currents radiates, but the magnitude of this radiation is small unless all the dimensions of the circuit approach the order of magnitude of a wavelength. However, since all harmonics of the fundamental may be present in a square wave, precautions must be taken to preclude induced voltages on adjacent circuits by stray electromagnetic fields.

The principal noise generator in a transistorized dc to dc switching converter is the power transformer, its pair of switching transistors, and the interconnecting wires. Each switching element separately conducts essentially square waves of current 180 degrees out of phase with each other at the transformer frequency. However, if the wires from the transformer to the semi-conductor switches are routed as pairs, the net current in the pair of wires will be some average dc with an ac component directly proportional to the dwell time between pulses and inversely proportional to the order of the harmonic. The induced field from this current can be further reduced by maintaining the shortest possible distance between the transformer and the transistors. Series line inductors

and shunt capacitors provide a low impedance current source at the transformer and a high impedance on the lines in order to contain the ac components in the vicinity of the switching.

The magnetic cores of the transformer, particularly of any saturating transformer, are noise generators since the B-H loop of the material used is not a monotonic function. Each inflection point on this loop is a potential source of broad band interference and electromagnetic radiation. These circuit devices are, by their very nature, "dirty" RFI elements which must be banished to isolated areas of the chassis to prevent contamination of "clean" input and output leads.

EVALUATION OF VARIOUS VOLTAGE BOOST REGULATION TECHNIQUES

By this criterion, the design approach for the main bus regulator can now be chosen. In applying these principles for RFI reduction, care must be taken in selecting the regulation technique to minimize the following:

1. Power core saturation.
2. Maximum peak and average currents switched by the power transistors.
3. The magnitude of ac voltages and currents in the main power flow paths.
4. Abrupt discontinuities in voltage or current waveforms.

Four basic voltage boost regulator circuits were evaluted. They are shown in figures 2a through 2d.

Figure 2a shows a boost circuit commonly known as the "flyback" regulator. In this circuit transistor Q1 is used to short inductor L1 across the incoming dc supply. During the time interval when energy is being stored in inductor L1, capacitor C1 must supply the energy required by the load. When Q1 is switched off, the energy stored in L1 is discharged to the load and to C1 through diode CR1. By time-ratio control of Q1, the average output voltage at C1 can be varied from slightly above supply level to a value several times higher.

Some major disadvantages of this circuit from an RFI standpoint are the following:

1. Q1 and CR1 must always carry and switch peak currents in excess of the dc load current.

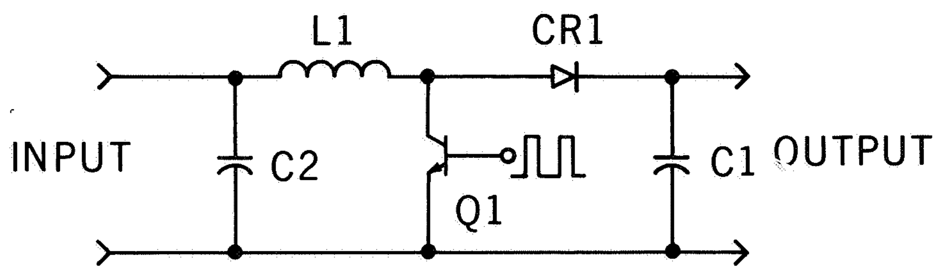


Figure 2a–Flyback Regulator

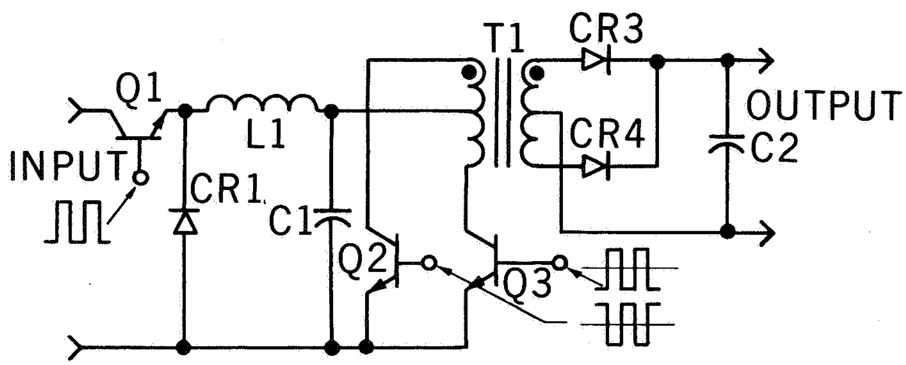


Figure 2b–Series Switch with DC to DC Converter

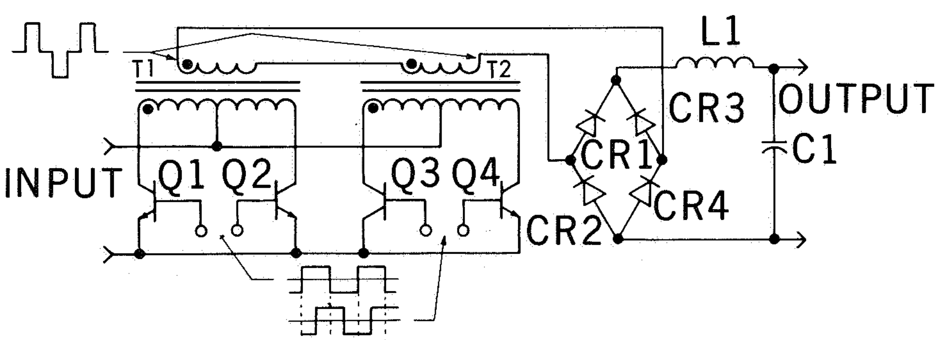


Figure 2c–Phasor Addition DC Regulator

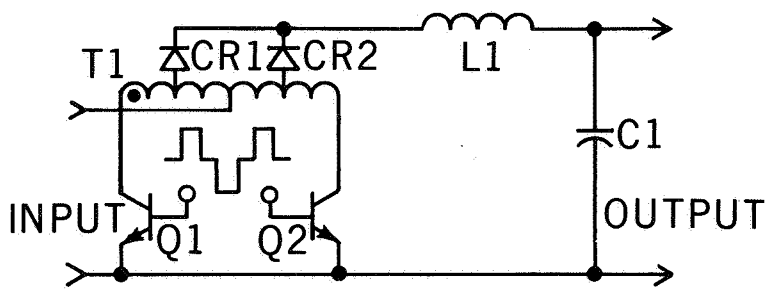


Figure 2d–Boost Transformer DC Regulator

2. Energy is transferred in the form of pulses within such a circuit, thus producing major RFI.

3. The ac peak-to-peak voltage (source of radiated RFI) at the input to CR1 is at least equal to and often greater than the supply voltage, depending upon the boost voltage required.

4. Current drawn from the source is in the form of high discontinuous pulses requiring large filters to prevent conduction into the source.

Figure 2b shows a simple switching regulator followed by a dc to dc converter. Transistor Q1 is "time-ratio-controlled" as an "on-off" switch to provide a variable-pulse-width square wave to the input of an averaging filter composed of L1 and C1. The output from the filter is a dc voltage whose level is a function of the "on" time, and the frequency of the power switch, and the voltage input. A pumpback diode CR1 is used to complete the path of current by the filter choke L1 to the load during Q1 "off" time. The output of the series switching circuit is then fed to the inverter, which boosts the voltage by transformer action. A bridge rectifier is used to obtain the desired dc level. Capacitor C2 is needed to filter the bridge output.

Some disadvantages of such a circuit are the following:

1. Components CR1 and Q1 (as with the preceding circuit) plus Q2 and Q3 must carry and switch peak currents in excess of the dc load current.

2. The ac peak-to-peak voltage at the input of CR1 is equal to the maximum input voltage.

3. Primary load current is always handled by two series semiconductors (Q1 or CR1, and Q2 or Q3).

4. Energy transfer in the form of pulses must occur from source to filter and load when Q1 is closed, and then from the filter to the load when Q1 is open.

5. The transformer in the inverter circuit must handle the full load power.

6. The ac component of voltage on the secondary of the inverter is twice that of the required dc output voltage.

7. Q1 is momentarily shorted to ground, producing high current transients at the instant of turn-on. This is due to the finite reverse recovery time of CR1.

Figure 2c shows a dc regulator composed of two power inverters. The two inverter outputs are applied to transformers T1 and T2. The transformer secondaries are connected in series for summing the inverter outputs. A diode bridge rectifies the summed waveform which is then fed to the input of an averaging filter. By varying the relative phase of the square waves driving the two inverters, the average value of the sum of the two outputs is varied. In this way, the dc input voltage can be increased or reduced as required. A particular advantage of this circuit is that CR1 and CR4 and alternately CR2 and CR3, are the only semiconductors which must carry the dc load current.

Some disadvantages of this circuit approach are the following:

1. The ac peak-to-peak voltage applied to the averaging filter is at least equal to the supply voltage.

2. As with the previous circuits, current drawn from the source is in the form of high discontinuous pulses resulting in conducted RFI problems.

Figure 2d shows a dc regulator which uses an inverter paralleled with the dc supply to provide a voltage boost. The switching action of Q1 and Q2 is complementary-controlled by pulse width modulation. The closing of Q1 or Q2 allows the input voltage to appear across the associated primary of T1. This voltage is coupled by auto-transformer action to the secondary by the turns ratio and represents a boost segment impressed upon the input voltage. A filter smooths the pulsating dc to the desired output level. By varying the boost voltage pulse width through control of the "on" times of Q1 and Q2, the average voltage at the output can be varied.

The following equations describe the operation of this boost circuit, assuming no series circuit losses and ideal transformer coupling:

$$E_{\text{Boost Inst.}} = E_{IN} \frac{N_S}{N_P}, \tag{1}$$

$$E_{OUT} = \frac{E_{\text{Boost Inst.}} T_{ON}}{T_{\text{Total}}} + E_{IN}, \tag{2}$$

$$I_{\text{Q1 (Q2) Inst.}} = I_L \frac{N_S}{N_P}, \tag{3}$$

$$I_{IN} = I_L + I_L \frac{N_S}{N_P} \frac{T_{ON}}{T_{TOTAL}}. \qquad (4)$$

Some advantages which this circuit offers are the following:

1. For the magnitude of boost voltage required in this application, the power transistors Q1 and Q2 carry and switch currents less than the load current. The magnitude is solely a function of the turns ratio, which, in turn, is set by the voltage boost required.

2. The inverter need be designed to provide only the boost power and not the entire load power. Accordingly, only boost energy is switched within the supply; thus, a major source of RFI is greatly reduced.

3. The ac peak-to-peak voltage applied to the averaging filter is only the boost component and not the full input voltage.

4. Diodes CR1 and CR2 are the only series semiconductors carrying full load current.

5. The pulse current drawn from the source is only that required by the inverter and not the full load current as with the previous circuit.

PART III

DESCRIPTION OF THE MAIN BUS REGULATOR

A block diagram of the main bus regulator is shown in figure 3a, while the circuit diagram with parts list appears in figure 3b. Figure 3c shows ideal voltage waveforms at various points in the circuit. A description of its operation follows:

Constant Frequency Square Wave Oscillator: A constant frequency, variable-pulse-width mode of operation was selected to enable precise filtering of the regulated output for sensitive loads. The operating frequency is established by a one-transformer, saturable-core transistor multivibrator. The frequency of operation is essentially constant, varying only by the percentage change of the output voltage (regulation) which is held to better than ±2%. The oscillator consists of resistors R5 and R6; diodes D10, D11 and D12; transistors Q5 and Q6; and transformer T4; its output is a 5 KHz square wave.

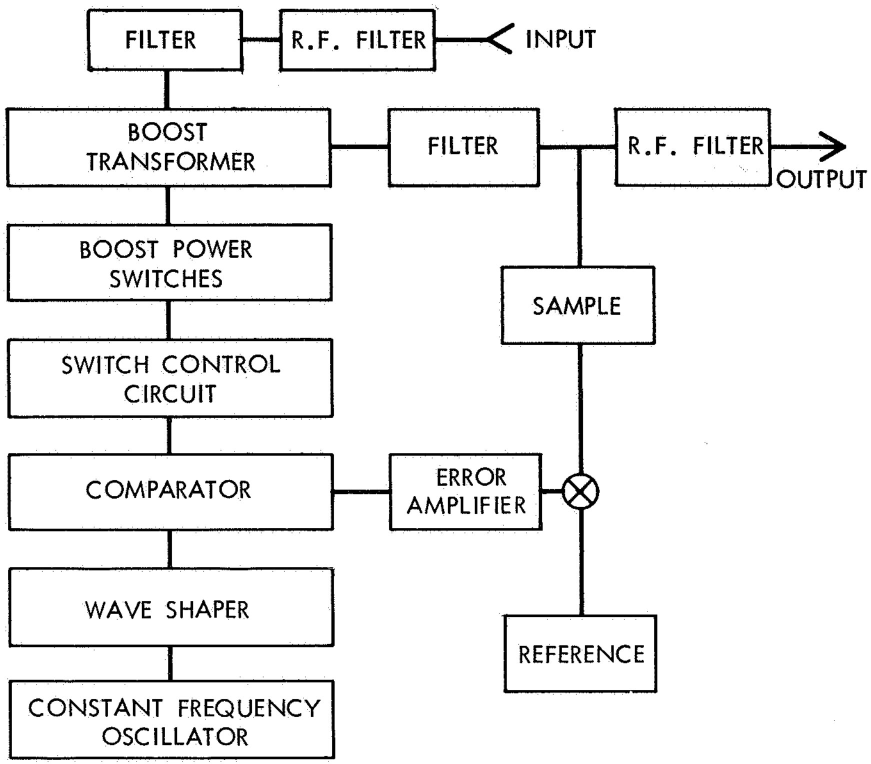


Figure 3a–Block Diagram of the Main Bus Regulator

A fixed voltage, determined by the output voltage, the transistor saturation voltage drop, and the winding resistance, is impressed upon the transformer primary windings. The winding is designed to withstand this fixed voltage for a constant period of time; after which core saturation results producing a 180 degree phase shift of the circuit operation. From Faraday's Law of Equation 5, the frequency of operation can be determined.

$$F = \frac{E \times 10^8}{4BNA} \tag{5}$$

where F = frequency in hertz

E = square wave voltage in volts

B = flux density at saturation in gauss

N = number of conductor turns

A = effective core cross-sectional area in cm^2

The turns ratio of base feedback turns to primary turns is chosen as equal to minimum gain at maximum load. This will insure that the switching transistors remain in saturation for the maximum oscillator load current.

Wave Shaper: The square wave generated by the transistor oscillator is integrated into a triangular waveform through a resistor (R3 or R4) and across capacitor C3. This RC time constant is chosen such that only the linear portion of the exponential rise is used. Center-tapped transformer T3 and diode D6 are provided to complete the circuit to ground.

Comparator: The constant frequency triangular wave reference is applied to the bases of a pair of common emitter npn transistors Q3A and Q3B. These

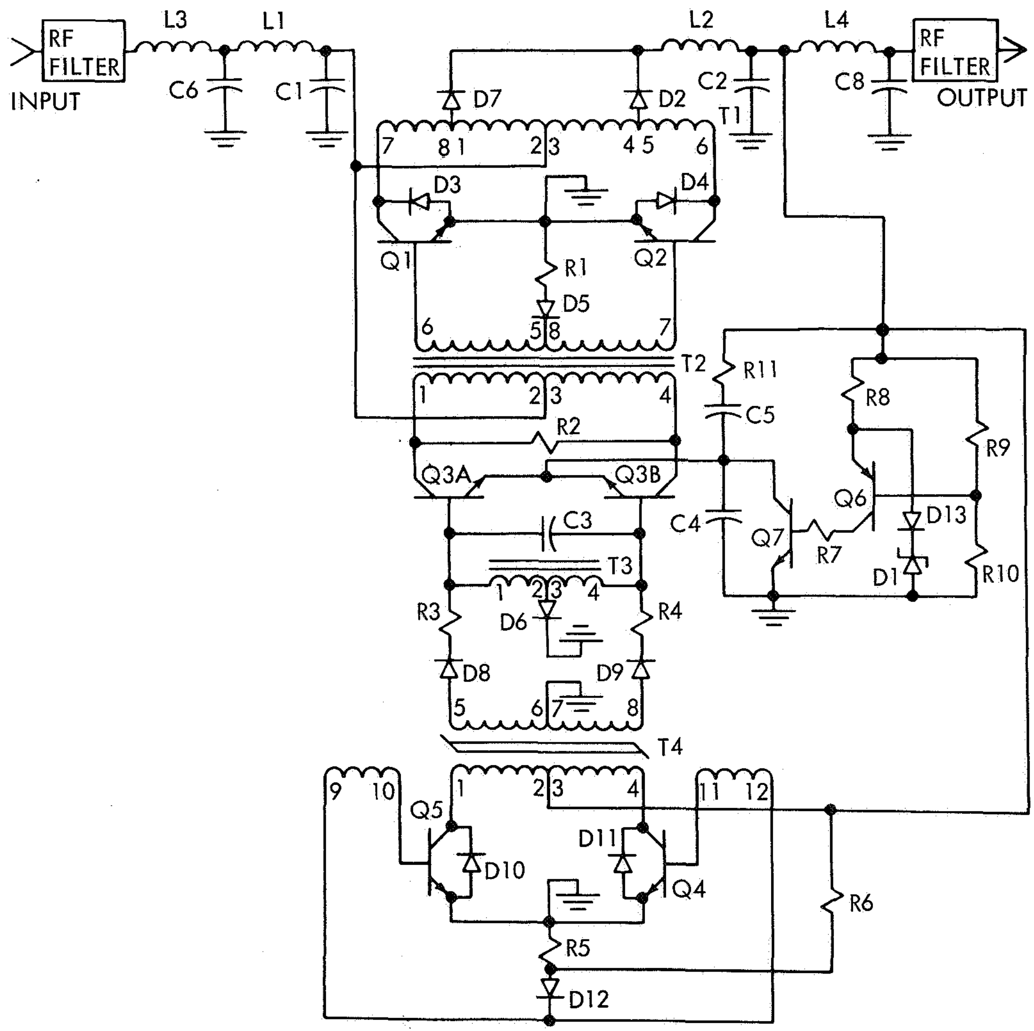


Figure 3b–Schematic of R.A.E. Main Bus Regulator

PARTS LIST FOR THE MAIN BUS REGULATOR

Transistors		Diodes	Capacitors		Resistors	
Q1	2N2812	D1-IN939B	C1-180μfds	30 Vdc	R1 - 10Ω	0.25W
Q2	2N2812	D2-U766-4	C2-360μfds	30 Vdc	R2 - 4.99K	0.125W
Q3A	MHD4456	D3-UTX-225	C3-0.047μfds	100 Vdc	R3 - 2K	0.125W
Q3B		D4-UTX-225	C4-0.35μfds	50 Vdc	R4 - 2K	0.125W
Q4	2N2034	D5-IN645	C5-2μ fds	100 Vdc	R5 - 1K	0.125W
Q5	2N2034	D6-IN3600	C6-100μfds	50 Vdc	R6 - 100K	0.125W
Q6	2N2904	D7-U766-4	C8-4μfds	100 Vdc	R7 - 3.5K	0.125W
Q7	2N2034	D8-IN3600			R8 - 1.8K	0.125W
		D9-IN3600			R9 - Sel.≈ 4.86K	0.125W
		D10-IN3600			R10- 4.75K	0.125W
		D11-IN3600			R11 = Sel.≈ 39Ω	0.25W
		D12-IN645				
		D13-IN3600				

Chokes

L1 - 85μh
36T AWG 15
55310-A2 Core

L2 - 525μh
56T AWG 16
55546-A2 Core

L3 - 10μh
11T AWG 17
55047-A2 Core

L4 - 80μh
24T AWG 17
55117-A2 Core

Transformers

T_1 - 6T5233-S1 Core
$N_{12} = N_{34}$ = 31T AWG 17
$N_{56} = N_{78}$ = 9T AWG 16

T_2 - 6T5515-S1 Core
$N_{12} = N_{34}$ = 328T AWG 31
$N_{56} = N_{78}$ = 131T AWG 27

T_3 - 17986P1000-47 Core
$N_{12} = N_{34}$ = 600T AWG 38

T_4 - 18236P1000-38 Core
$N_{12} = N_{34} = N_{56} = N_{78}$ = 192T AWG 34
$N_{9-10} = N_{11-12}$ = 27T AWG 34

RF Filters

1200 - 025   10A, 50 Vdc

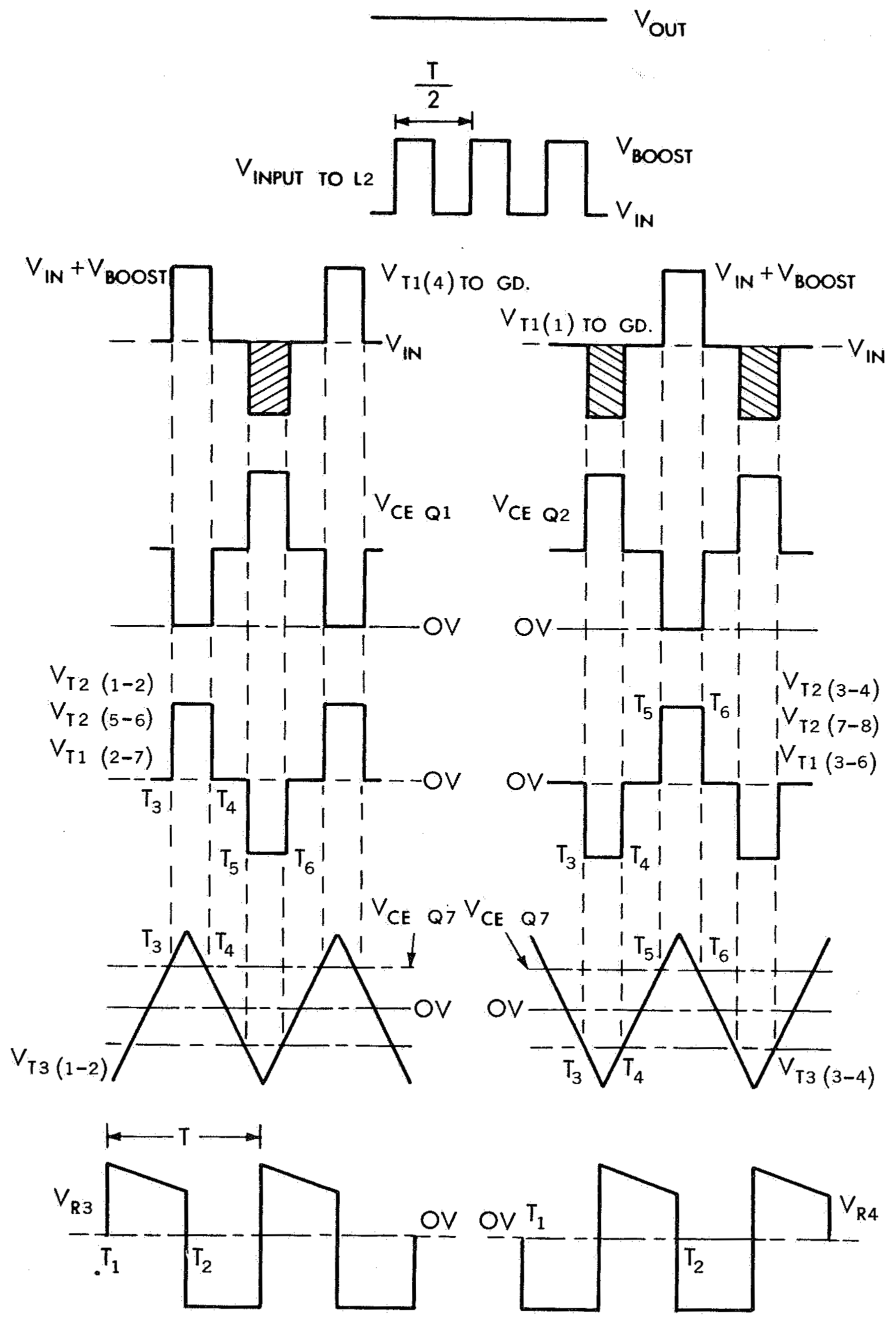


Figure 3c—Ideal Waveforms of the Main Bus Regulator

transistors have a common base voltage but displaced 180 degrees in time. Since both transistor bases and emitters have a common ground reference, the conduction period of either transistor is a function of the time the triangular base voltage exceeds the common emitter voltage less the base-emitter drop. The voltage at the common emitter point is a function of the error signal resulting from the current sharing action of a transistor shunt-capacitor pair (Q7 and C4).

Figure 4a shows the simplified equivalent regulation circuit with associated transistor switches. An error signal in the form of an increasing base drive for

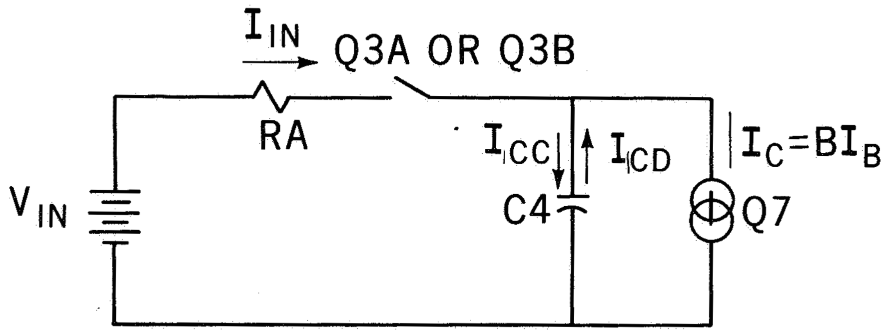
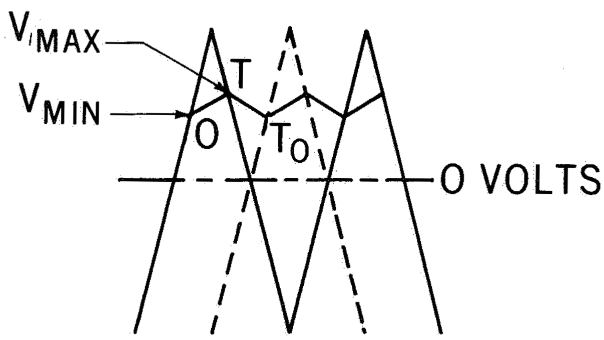


Figure 4a–Simplified Equivalent of the Regulation Control Circuitry



SOLID TRIANGULAR WAVE: VOLTAGE BASE TO GROUND OF Q3A
DOTTED TRIANGULAR WAVE: VOLTAGE BASE TO GROUND OF Q3B
VOLTAGE ACROSS C4 IS IMPRESSED UPON THESE WAVEFORMS

Figure 4b–Waveforms Showing Steady State Condition

Q7 is provided whenever the output falls. The greater conduction of Q7 lowers the sampling level on the constant-frequency triangular waveform driving the bases of Q3A and Q3B, thus increasing their "on" time. This increased "on" time is transformer-coupled to the series switching transistors in an attempt to increase the output voltage.

A close look at the regulation scheme shows it to be a function of the voltage of C4 and the base drive of Q7. The current source for charging C4 and providing collector current for Q7 is relatively constant since, from the equivalent circuit, RA is much larger than any other series resistance in this path. Whenever transistor switch Q3A or Q3B is closed, the constant current which flows must divide to form a charge current to C4 and a collector current for Q7. During the time Q3A and Q3B are open, capacitor C4 must supply the collector current of Q7 (as required by its base drive).

Assuming a steady state condition as shown by the diagram in figure 4b, analysis of operation can be derived giving the duty cycle of the power switches, Q1 or Q2 (required to give the proper boost voltage for the desired output). Equation 12 gives that result. The derivation follows:

$$RA = \frac{\left(\frac{N_P}{N_S}\right)^2 R1 \cdot R2}{\left(\frac{N_P}{N_S}\right)^2 R1 + R2} \tag{6}$$

$$V_{max} - V_{min} = \frac{1}{C4}\left[\frac{V_{IN} - V_{min}}{RA} - BI_B\right] T_0 \tag{7}$$

$$V_{max} - V_{min} = \frac{1}{C4} BI_B (T - T_0) \tag{8}$$

$$\frac{1}{C4} BI_B (T - T_0) = \frac{1}{C4}\left[\frac{V_{IN} - V_{min}}{RA} - BI_B\right] T_0 \tag{9}$$

$$\frac{BI_B T - BI_B T_0}{T_0} = \frac{V_{IN} - V_{min}}{RA} - BI_B \tag{10}$$

$$\frac{BI_B T}{T_0} = \frac{V_{IN} - V_{min}}{RA} \tag{11}$$

$$\frac{T_0}{T} = \frac{RA \cdot BI_B}{V_{IN} - V_{min}} \tag{12}$$

where

T_0 = time Q1, Q3A or Q2, Q3B are closed.

T = total time Q1, Q3A or Q2, Q3B could be closed.

RA = series resistance defined by Equation 6.

V_{IN} = input voltage to be regulated.

V_{min} = initial capacitor charge voltage prior to closing of Q3A or Q3B.

B = transistor Q7 current gain factor = I_C/I_B

I_B = base current of Q7 which is proportional to error signal obtained from sensing output voltage.

$\frac{N_P}{N_S} = \frac{\text{Primary turns of T2 (1 - 2 or 3 - 4)}}{\text{Secondary turns of T2 (5 - 6 or 7 - 8)}}$

<u>Switch Control Circuit:</u> The pulse width modulated switch control circuit is composed of transformer T2, diode D5, and resistors R1, R2. A transformer (T2) coupled signal provides base drive to the transistor switches causing them to remain in the closed or saturated state for the duration of the "on" pulse, thus allowing the source voltage to appear across the primary of T1. The maximum conduction time of either of the complementary transistor switches is 180° due to the transformer base drive circuit mode of control. Resistor R1 is used to limit the base drive current to the power transistor switches, while R2 is provided to improve drive waveform fall times.

Boost Power Switches: Power switches Q1 and Q2 control the signal to the boost transformer for voltage step-up. These switches are not in the main power line but handle only the boost power.

Reliable operation of the power switches was insured by selection of parts with adequate breakdown voltage relatively high current capability, and fast switching. The device to be used here as a switch is a silicon NPN power transistor, 2N2812. Diodes D3 and D4 are used to provide a path for reactive energy pumpback.

Boost Transformer: Whenever either transistor switch closes, the input voltage is impressed across the primary of T1 for the duration of the closure. This voltage is coupled by auto-transformer action to the secondary and added to the input for the switch "on" time duration. The primary current required is the magnetizing current plus the load current coupled back to the primary by the turns ratio. Thus, the primary current which must be handled by the transistor switches is a fixed value, determined by the turns ratio but less than the load current by the turns ratio. This ratio is 1.30 to 1, primary turns to secondary turns, since the transformer is designed to provide a boost of 8.5 volts with a minimum input voltage of 11 volts and complementary switches, Q1 and Q2, each alternately closed for 180°, the longest period of time possible.

To keep the transformer from excursions into deep saturation with resulting high current spikes, supermalloy was selected as the core material, while bifilar windings were used to minimize the leakage reactance.

Filter (Output): The output of the boost transformer, which is a double frequency waveform, is rectified by diodes and fed to an LC filter. This filter need only handle the boost voltage segment and smooth it to a dc voltage of low ripple.

In the design of this filter, a criterion for conventional power supply filter design was considered: that unidirectional current flow be maintained through the series inductor at all times. This rule of thumb is used for two reasons: (1) To prevent the apparently high inherent regulation of the power supply from appearing at its output terminals, and (2) For the realistic requirement of controlling the ratio of peak-to-average current through the series element for protection of semiconductors and good thermal efficiency.

If the criterion for critical inductance is imposed, the choke must be designed so that the peak ac current (over or under average) through the inductor does not exceed the average value determined by the nominal output voltage and maximum load resistance (minimum load current).

A derivation of the critical inductance equation for the boost regulator follows: Let

E_f = input voltage to filter in volts,

E_i = input voltage in volts,

E_o = output voltage in volts,

I_{ac} = current of filter in amperes,

I_o = output load current in amps at maximum load resistance,

k = duty cycle of the power switches Q1 or Q2,

L = inductance in henries,

L_C = critical inductance in henries,

n = harmonic term number,

ω = the output ripple frequency in radians/second,

N = turns ratio N_S/N_P of T_1,

R_o = maximum load resistance in ohms.

The pulsating, unidirectional voltage delivered by the switching transistors may be represented by the Fourier series:

$$E_f = E_i \left[1 + Nk + \frac{2}{\pi} \frac{(\sin nk\pi \cos n\omega t)}{n} \right] \qquad (13)$$

$$I_0 = \frac{E_i + E_i Nk}{R_0} \qquad (14)$$

If the impedance of the shunt combination of load resistance and output capacity is small compared to the impedance of the inductor at the ripple frequency, then

all the ac voltage will appear across the inductor and the ac current can be found from

$$I_{ac} = \frac{E_{ac}}{\omega L} = \frac{\left[\frac{2E_i}{\pi} \frac{\sin nk\pi \cos n\omega t}{n}\right]}{\omega L} \tag{15}$$

Applying critical inductance criteria gives:

$$I_{ac} \leqq I_o \text{ and} \tag{16}$$

$$\frac{2E_i \sin k\pi \cos \omega t}{\pi\omega L} \leqq \frac{E_i (1 + Nk)}{R_o} \text{ at } n = 1. \tag{17}$$

Simplifying with peak currents occurring at

$$\cos \omega t = \pm 1 \quad \omega t = 0, \pi, 2\pi, n\pi$$

we find

$$L = \frac{2R_o \sin k\pi}{\pi\omega (1 + Nk)} \tag{18}$$

Determining k value at which maximum rate change of current occurs:

$$V_L = (E_i + E_i N - E_o) = L \frac{d_i}{d_t}, \tag{19}$$

$$L = \frac{\Delta t \; [E_i (1 + N) - E_o]}{\Delta i}, \tag{20}$$

$$E_o = E_i (1 + Nk). \tag{21}$$

Substituting Equation (21) into Equation (20) gives:

$$L = \frac{\Delta t}{\Delta i} [E_i (1 + N) - (E_i \{1 + Nk\})]. \tag{22}$$

Simplifying Equation (22) gives:

$$L = \frac{\Delta t}{\Delta i} [E_i N (1 - k)] \tag{23}$$

and, since $\Delta t = tk$,

$$\Delta i = \frac{t E_i N (k - k^2)}{L} \tag{24}$$

Differentiating Equation (24) with respect to k and equating to zero will give the k value desired:

$$\frac{d}{dk} \frac{\Delta i L}{t E_i N} = \frac{d}{dk} (k - k^2) = 1 - 2k = 0, \tag{25}$$

Therefore

$$k = \frac{1}{2}.$$

Substituting this value into Equation (18) gives:

$$L_c = \frac{2 R_0}{\pi\omega \left(1 + \frac{N}{2}\right)} \tag{26}$$

Since $\omega = 2\pi f$, we find that

$$L_c = \frac{R_0}{\pi^2 f \left(1 + \frac{N}{2}\right)}. \tag{27}$$

Sample-Reference-Error Amplifier: A resistance-divider network provides a sample of the output which is compared through a transistor to a constant voltage reference established by a zener diode element. Whenever an unbalance exists such as would be the case with an output voltage below the regulation set level, an increased current flows in the base circuit, forcing the transistor Q6 to conduct more fully. This results in a greater conduction of Q7, which lowers the sampling level on the triangular waveform in an attempt to increase the output voltage.

The reference element employed for sensing is D1. Diode D13 is used for temperature compensation of Q6. The zener current needed to establish the constant reference is obtained through R8. C5 and R11 form an auxiliary feedback path to provide fast response to transient load and input line changes. Whenever the output voltage changes, a corresponding error signal is passed directly to the emitters of Q3A and Q3B in an attempt to instantaneously change the voltage at this point, and thus change the "on" time or pulse width of the power switches through the drive networks.

Filters (Input): A double section LC filter is used at the input to the boost regulator to maintain low ripple voltage and current and prevent feedback onto the input power line.

Filter (RF Input & Output): An rf filter is used at both the input and the output of the pre-regulator to prevent high frequency ac components of ripple, which are not filtered by the main filters, from reflecting into the input and output lines. The main filters cannot remove these high frequency components due to their non-ideal characteristics, such as the presence of capacitor series resistance (ESR) and inductance due to the construction of the capacitor. The filter choke series resistance and distributed capacitance also prevent good high-frequency filtering. The RF filter is specially designed to reduce the effect of these non-ideal characteristics. An additional filter is used at the output to remove the medium and high frequency harmonics present in the ripple waveform across the main output filter capacitors. The filter reshapes this ripple to a sine wave of low harmonic content. This filter was required to minimize the transfer of conducted noise into the load.

PERFORMANCE

The performance characteristics of the main bus regulator are shown in figures 5 through 9. The voltage regulation and efficiency are plotted as a function of input voltage variance from 12 to 17 volts, simulating possible operating points on a solar-array-battery composite power curve. The output current levels chosen for these plots, 0.25, 0.5, 1.0, and 2.5 amperes, represent power levels of 4.5, 9, 18, and 45 watts, respectively. Also plotted are curves

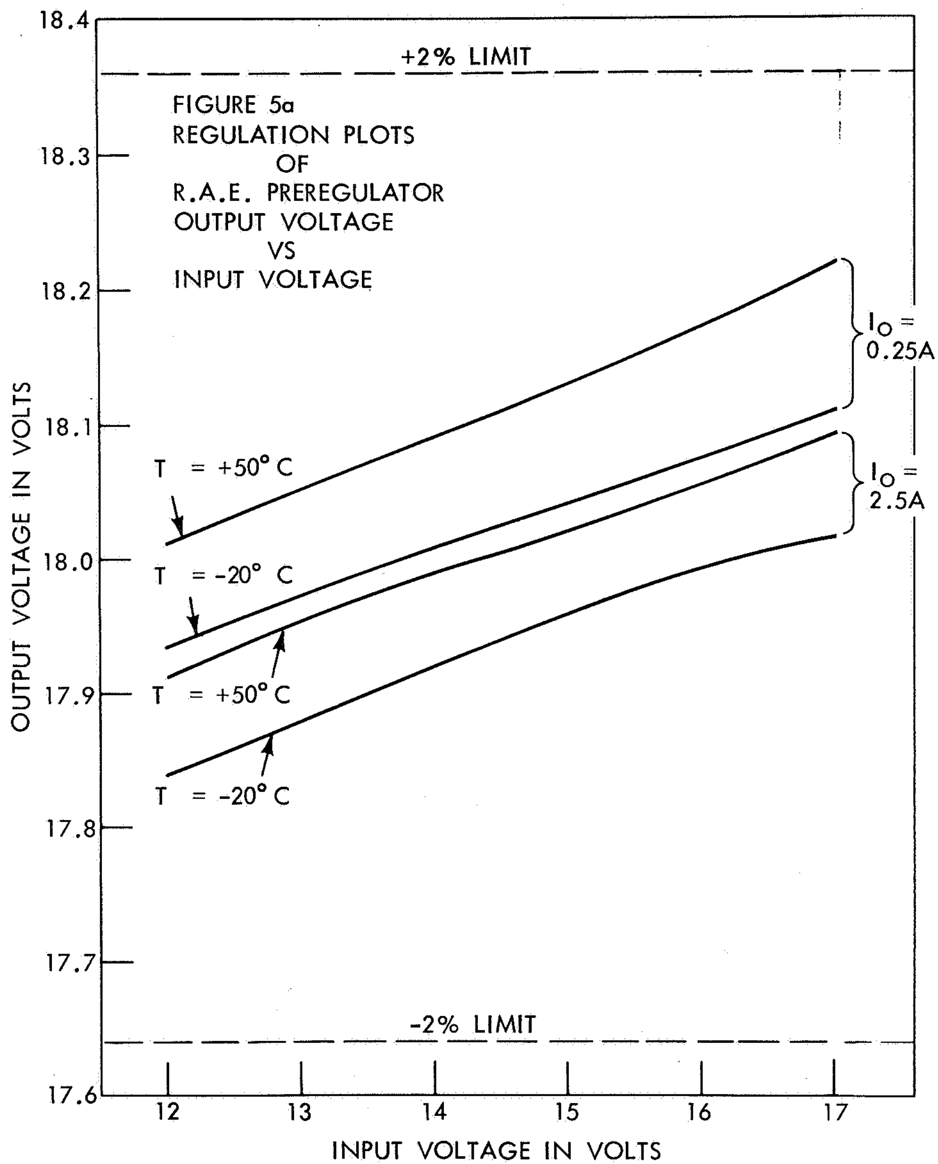


Figure 5a–Regulation Plots of RAE Pre-Regulator Output Voltage vs. Input Voltage

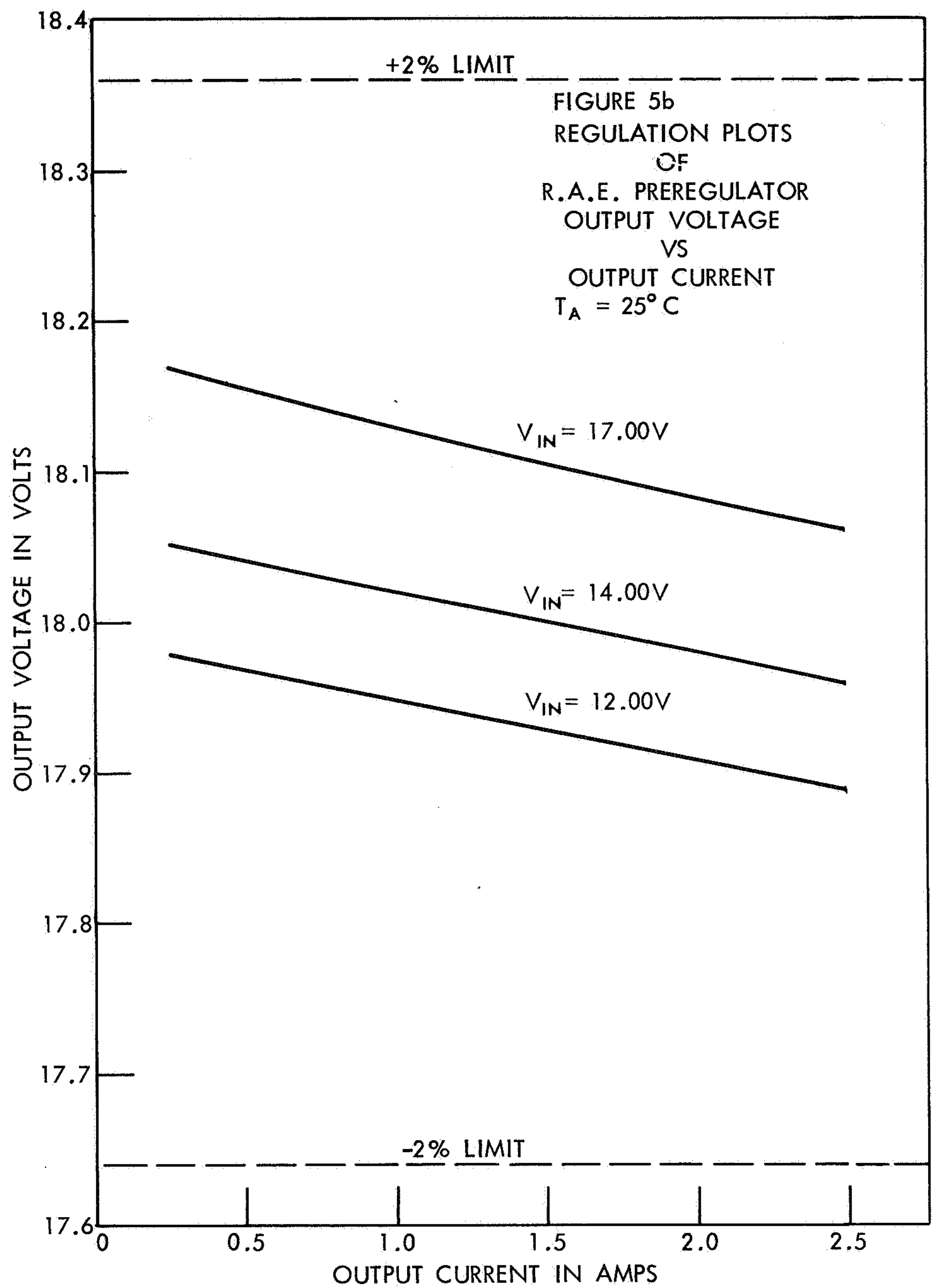


Figure 5b–Regulation Plots of RAE Pre-Regulator Output Voltage vs Output Current, T_A = 25°C

or radiated and conducted noise levels versus frequency. Photos of the steady state output ripple and the transient response of the regulator to step input and step load change are shown in figures 7, 8a and 8b, respectively.

Static Regulation: From the curves of figures 5a and 5b, it can be seen that the regulator has good load regulation, less than 0.6%, while the change due to temperature is also less than 0.6%. Input voltage variation produced the greatest change, approximately 1%. The total overall regulation due to all specified conditions is 2.2%, which is well within the limit band of 4% (±2%).

Efficiency: The regulator efficiency varies from a minimum of about 84% at a load current of 0.25 ampere and an input voltage of 12 volts to a maximum of 93% at a load current of 1.25 amperes and input voltage of 17 volts. The principal losses of the voltage boost regulator are in the forward dissipation of the boost diodes and the conduction dissipation and switching losses of the controlled transistors. With no load applied to the regulator, 400 milliwatts of power loss is attributed to the control and sensing circuitry.

From a close look at these curves (figures 6a and 6b), it can be seen that the lowest efficiency results at minimum load. This occurs since the constant control power loss of 0.4 watt is now significant when compared to the average output power of 4.5 watts. At loads of 0.5 ampere (9 watts) and above to 2.5 amperes (45 watts), the efficiency ranges from 88.5-93%. Note that as the load increases to its maximum value, the efficiency reaches a maximum and then decreases below that value. This is due to the nonproportional effect of the forward conduction and transistor switching losses at these higher load currents. For the nominal value of 1.25 amperes, the efficiency is very nearly at its maximum value.

Output Ripple: The maximum ripple of 80 millivolts occurs at an input of 14 volts and a load of 2.5 amperes. It is at this condition that the greatest rate of change of current occurs in inductor L2. Figure 7 shows the waveform of the ripple at this condition. Note that this waveform is a sinusoid of low harmonic content. The ordinary ripple waveform resulting from a switching regulator with LC output filter contained high frequency harmonics of appreciable value causing excessive conducted RFI. To alleviate this problem, an LC filter (L4 and C8) was added, resulting in a reshaping of the waveform into a sinusoid.

Dynamic Regulation: The transient response of the regulator to line and load changes is shown in the series of photographs of figures 8a to 8f. For the response to input voltage change, a 5-volt step change (12-17-12 volts) with rise and fall times less than 2 milliseconds was applied to the regulator input. This conditions represents the type of voltage excursion which results from the non-sun-oriented solar cells of a spin-stabilized satellite. The output voltage change that occurred was 0.35 volts, which is about the unit's static regulation as shown in figure 5b. Thus, for this step input change, the output response was rather good, exhibiting very little over- or undershoot.

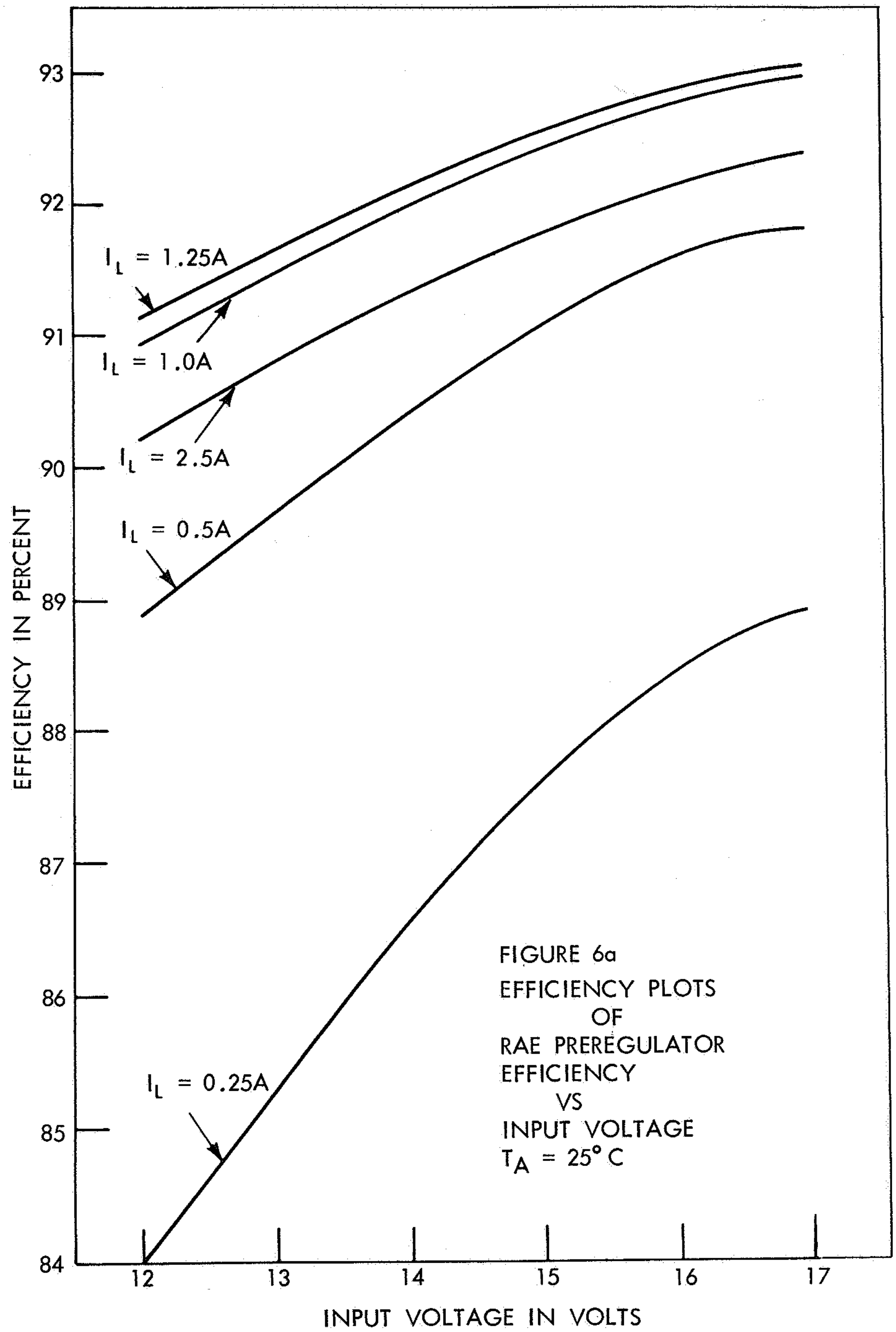


Figure 6a–Efficiency Plots of RAE Pre-Regulator Efficiency vs. Input Voltage, T_A =25°C

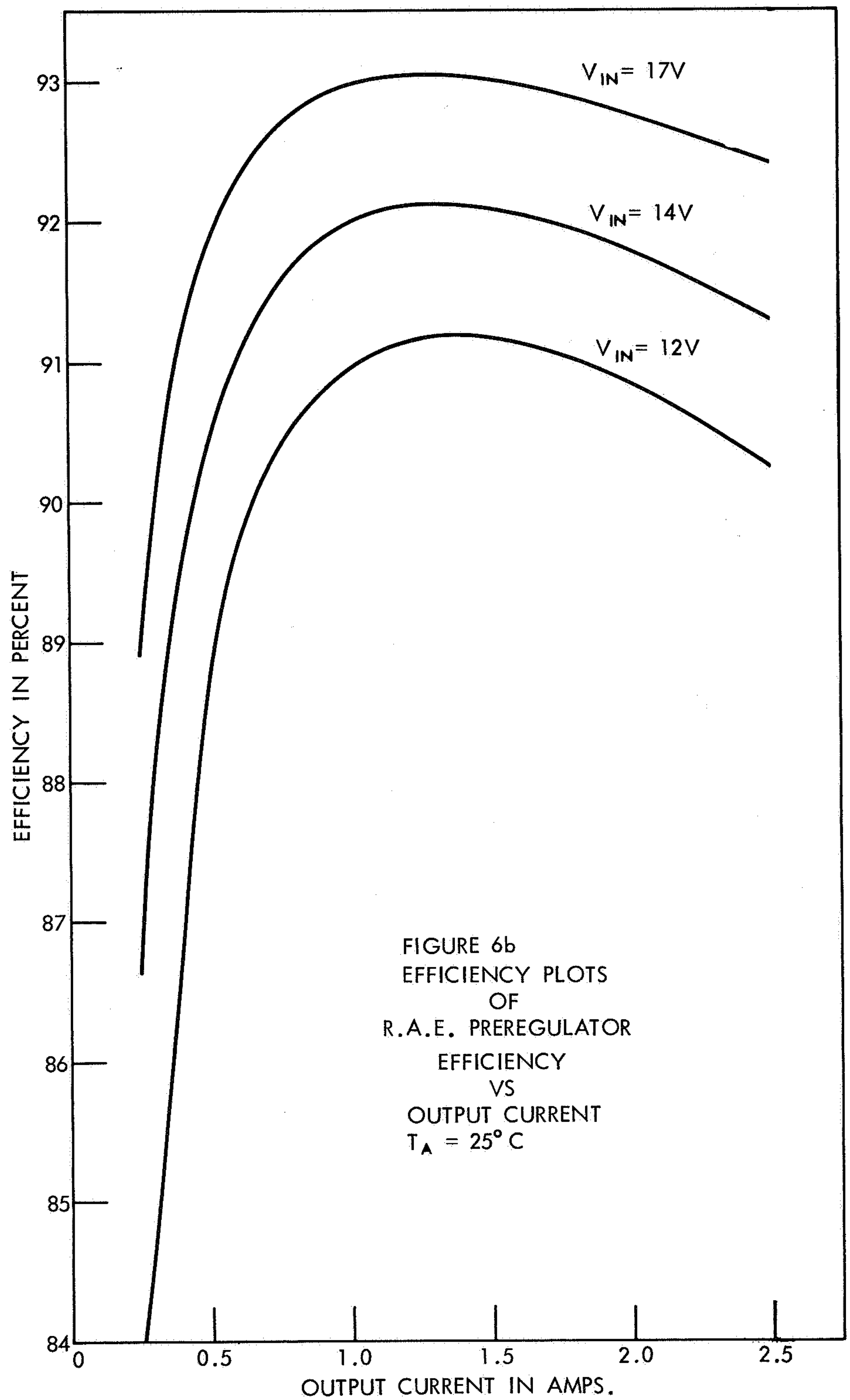
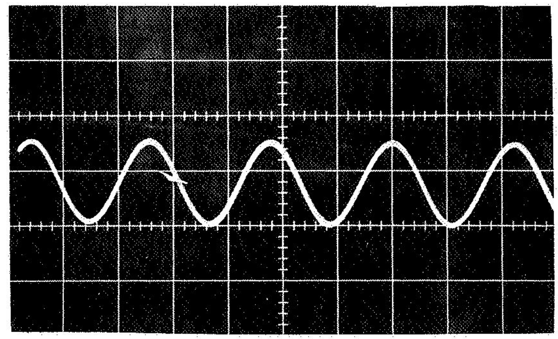


Figure 6b–Efficiency Plots of RAE Pre-Regulator Efficiency vs. Output Current, T_A =25°C

Figure 7–Photograph of Output Ripple of the Pre-Regulator, V_{IN} = 14V; V/cm = 50 MV; I_{LOAD} =2.5A; T/cm =50μS.



For the response to load change, a steady state load of one ampere was chosen, while a step of one ampere with rise and fall times less than 5 microseconds was the dynamic load applied to the output. The application of this load resulted in an undershoot of 3 volts (16.6%) with recovery to within the regulation range taking 0.6 millisecond. The removal of this load resulted in an overshoot of 3.2 volts (17.8%) with recovery to within the regulation range taking 0.8 millisecond. The response of the regulator to load change is considered good and is within the desired limits.

Figures 8c, d, e and f are oscillographs showing the output voltage, instantaneous load change, and the collector to emitter voltage of one of the power switches. From a close look at these photographs, you will see that the regulator will respond to correct the output, which has undergone a deviation from the nominal due to the applied load or line change, in less than the time of a half cycle of the fundamental frequency which is 5K hertz.

With the addition of the RF filter composed of L4 and C8, the transient response characteristics of the regulator were significantly changed. The oscillographs of figures 8g through 8i show the response of the regulator to the one ampere step load change with the filter L4 and C8 and RF output filter removed. Note that the output voltage does not exhibit the damped sinusoidal oscillation as with the previous circuit. Also note that the voltage over and undershoots are within the static regulation limits of ±2%. Thus we can see that while the filter provides significant harmonic suppression, it does this at the expense of transient response by effectively decoupling the regulator to some degree from the load during this transient interval.

<u>RFI:</u> The RFI characteristics of the main bus regulator are shown in the graphs of figures 9a and 9b. Plotted in these graphs are broadband-conducted interference and broadband-radiated interference versus frequency, as obtained by applying the applicable procedure in MIL-I-6181-D. A load of 1.75 amperes was chosen for these tests since the maximum interference occurred at this load.

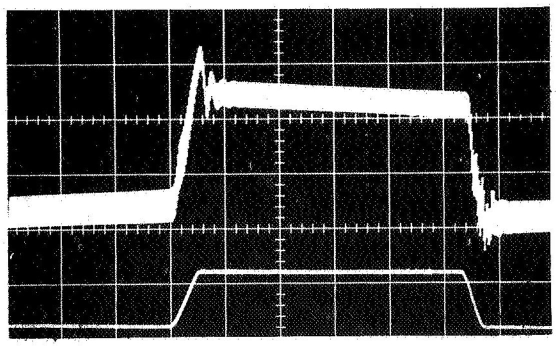


Figure 8a–Photograph of the Transient Response of the Prereg. to Step Input Voltage Change.
Upper Trace: $V_{OUT} = 0.1V/cm$
Lower Trace: $V_{IN} = 5V/cm$
$T/cm = 5$ ms; $I_{LOAD} = 1.0A$

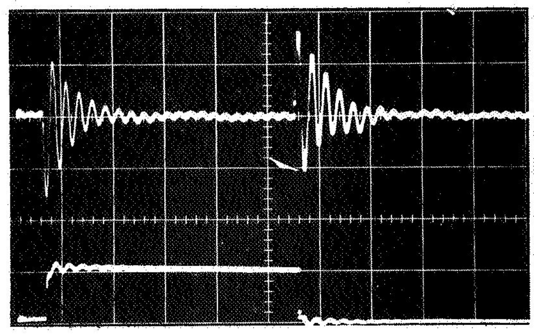


Figure 8b–Photograph of the Transient Response of the Prereg. to Step Load Change.
$V_{IN} = 14V$; $I_{LOAD} = 1.0A$
Upper Trace: $V_{OUT} = 2V/cm$
Lower Trace: $I_{LOAD} = 1.0A/cm$
$T/cm = 0.5$ ms

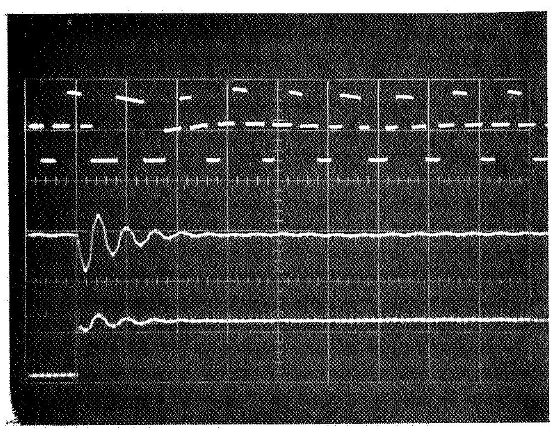


Figure 8c–Photograph of the Transient Response of the Prereg. to Step Load Change (Load Application).
$V_{IN} = 14V$; I_L Steady State = 1A
Upper Trace: V_{CE} of Q1 = 20V/cm
Middle Trace: $V_{OUT} = 5V/cm$
Lower Trace: $I_{LOAD} = 1A/cm$
$T/cm = 0.2$ ms

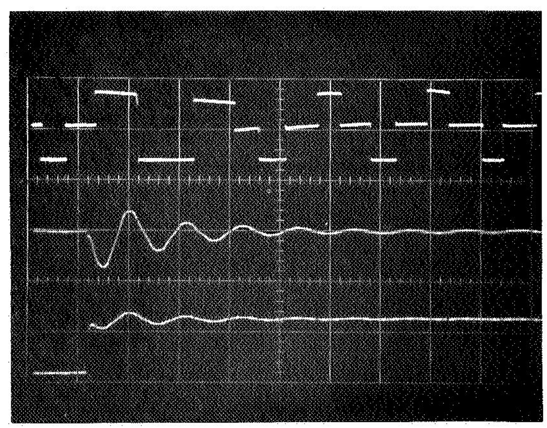


Figure 8d–Expanded trace of Figure 8c with $T/cm = 0.1$ ms

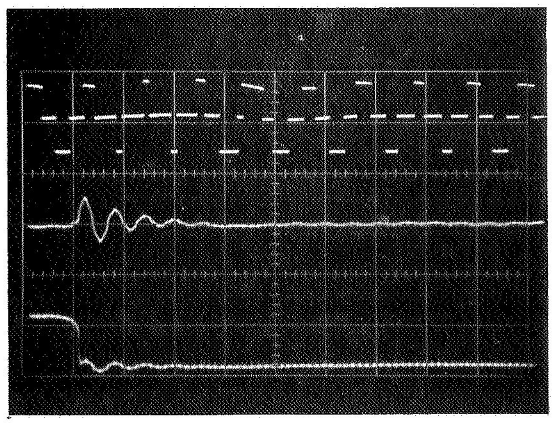


Figure 8e—Photograph of the Transient Response of the Prereg. of Step Load Change (Load Removal).
V_{IN} = 14V; I_L Steady State = 1A
Upper Trace: V_{CE} of Q1 = 20V/cm
Middle Trace: V_{OUT} = 5V/cm
Lower Trace: I_{LOAD} = 1A/cm
T/cm = 0.2 ms

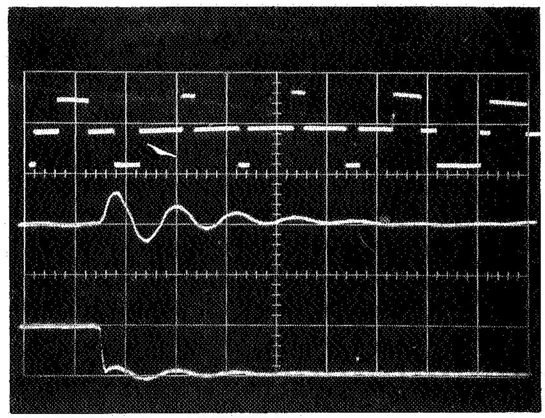


Figure 8f—Expanded trace of Figure 8e with T/cm = 0.1 ms.

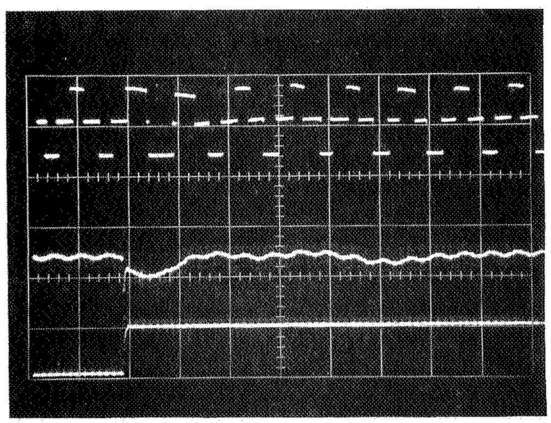


Figure 8g—Photograph of the Transient Response of the Prereg. without filter L4 and C8 (Load Application).
V_{IN} = 14V; I_L Steady State = 1A
Upper Trace: V_{CE} Q1 = 20V/cm
Middle Trace: V_{OUT} = 0.5V/cm
Lower Trace: I_{LOAD} = 1A/cm
T/cm = 0.2 ms

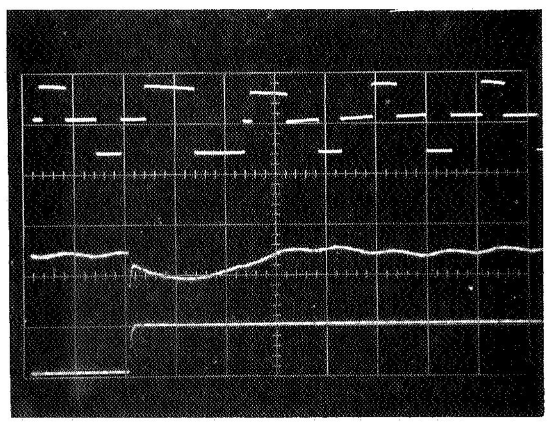


Figure 8h—Expanded trace of Figure 8g with T/cm = 0.1 ms.

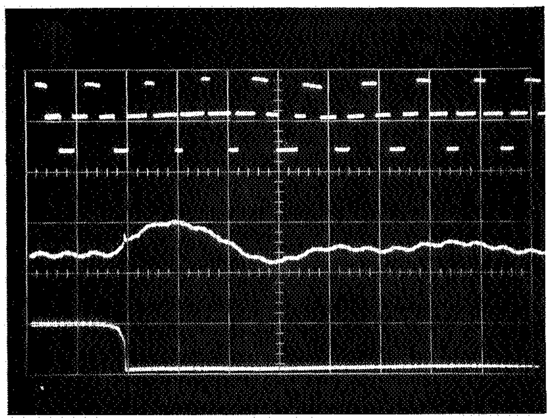


Figure 8i—Photograph of the Transient Response of the Prereg.without filter L4 and C8 (Load Removal).
V_{IN} = 14V; I_L Steady State = 1A
Upper Trace: V_{CE} Q1 = 20V/cm
Middle Trace: V_{OUT} = 0.5V/cm
Lower Trace: I_{LOAD} = 1A/cm
T/cm = 0.2 ms

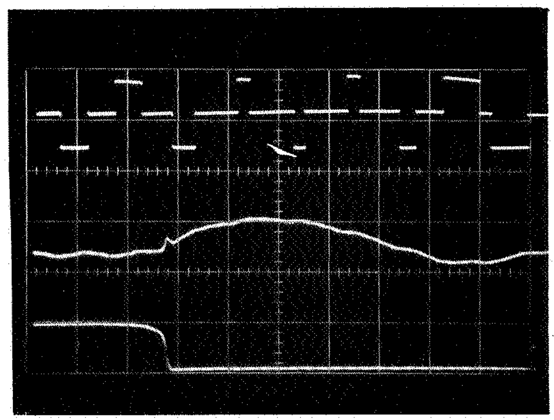


Figure 8j—Expanded trace of Figure 8i with T/cm = 0.1 ms.

Narrow band (cw) interference was considerably lower than broadband interference and was hardly detectable over the frequency range of concern.

Inspection of the conducted RFI graph shows that interference is present from 0.15 to 0.8 MHz and that a peak noise, including ambient, results at 0.6 MHz (approximately 0.38 microvolt). From 0.8 MHz to 10 MHz, no interference above the ambient noise level was detectable. Approximate dbMC values of noise, neglecting the variation with frequency of the instrument bandwidth, are shown for comparison to the military specification along with microvolts on the Y axis.

The graphs of radiated interference show a maximum of 0.2 microvolt between 0.15 and 0.2 MHz, while no noise above ambient was detectable from 0.3 to 10 MHz. In order to get some interference readings for this test, the antenna (VR 105) distance from the unit had to be decreased to 1 inch at the place of worst radiation. This data indicate that the generated interference was effectively contained within the unit.

MECHANICAL ASPECTS

Photos of the RAE main bus regulator package are shown in figures 10a and 10b. The overall size of the package is 5" × 7" × 3-1/4", occupying a volume of

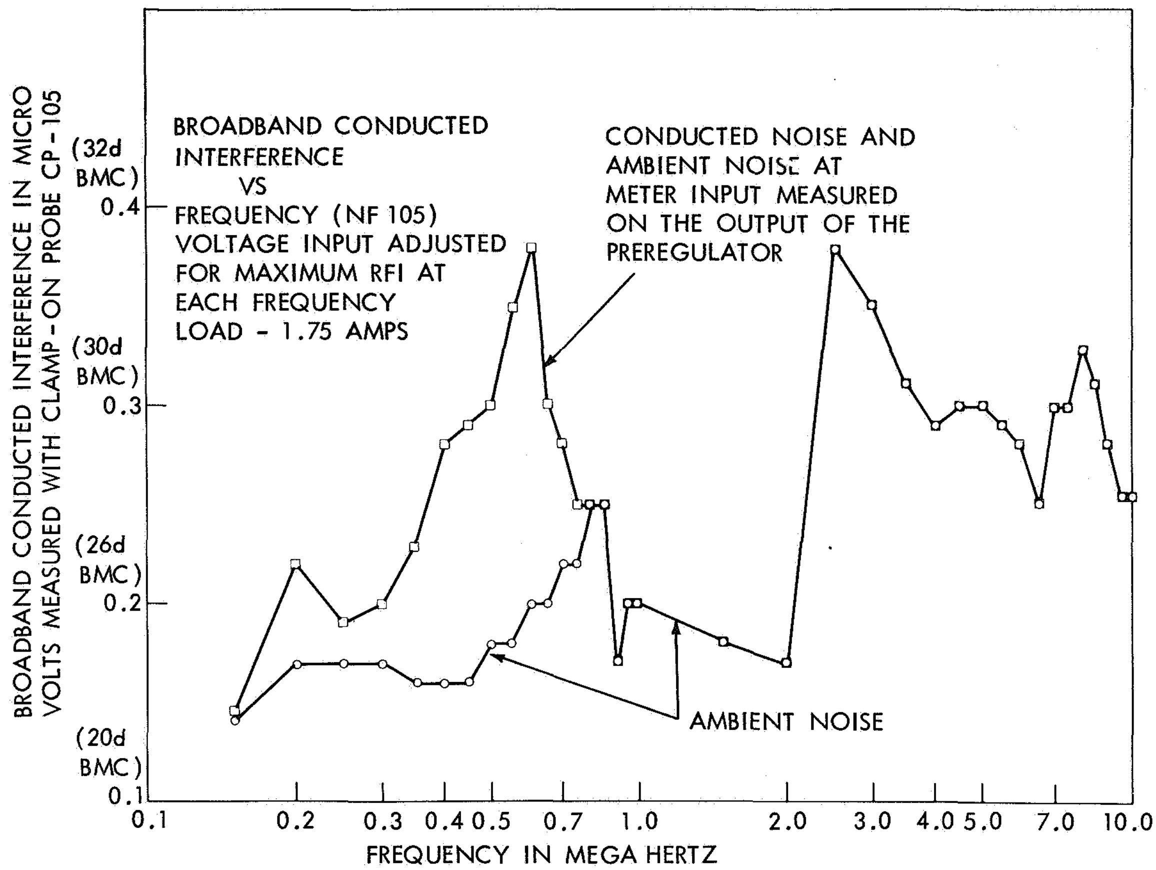


Figure 9a—Plots of conducted RFI of RAE Pre-Regulator

114 cu. in (housing two regulators). The total weight of the package is 3.8 pounds.

The chassis for the unit was milled from a solid block of aluminum and gold-plated for protection against corrosion and for good surface contact. Cover plates with screws placed on approximately 1-1/2 inch centers were used to seal the package and prevent RF leakage. The unit was divided into seven basic sections: Three per regulator (two redundant regulators enclosed) and a section for the connector and harness. The sectional divisions were used to provide functional isolation and RF shielding. The control, sensing, and reference oscillator circuitry were housed in one section, the input and boost circuitry in another, the output circuitry in still another, and the connector and harness in the remaining type of section.

Two basic types of packaging techniques were used in the mechanical design of the unit. The large components, such as chokes, transformers, power

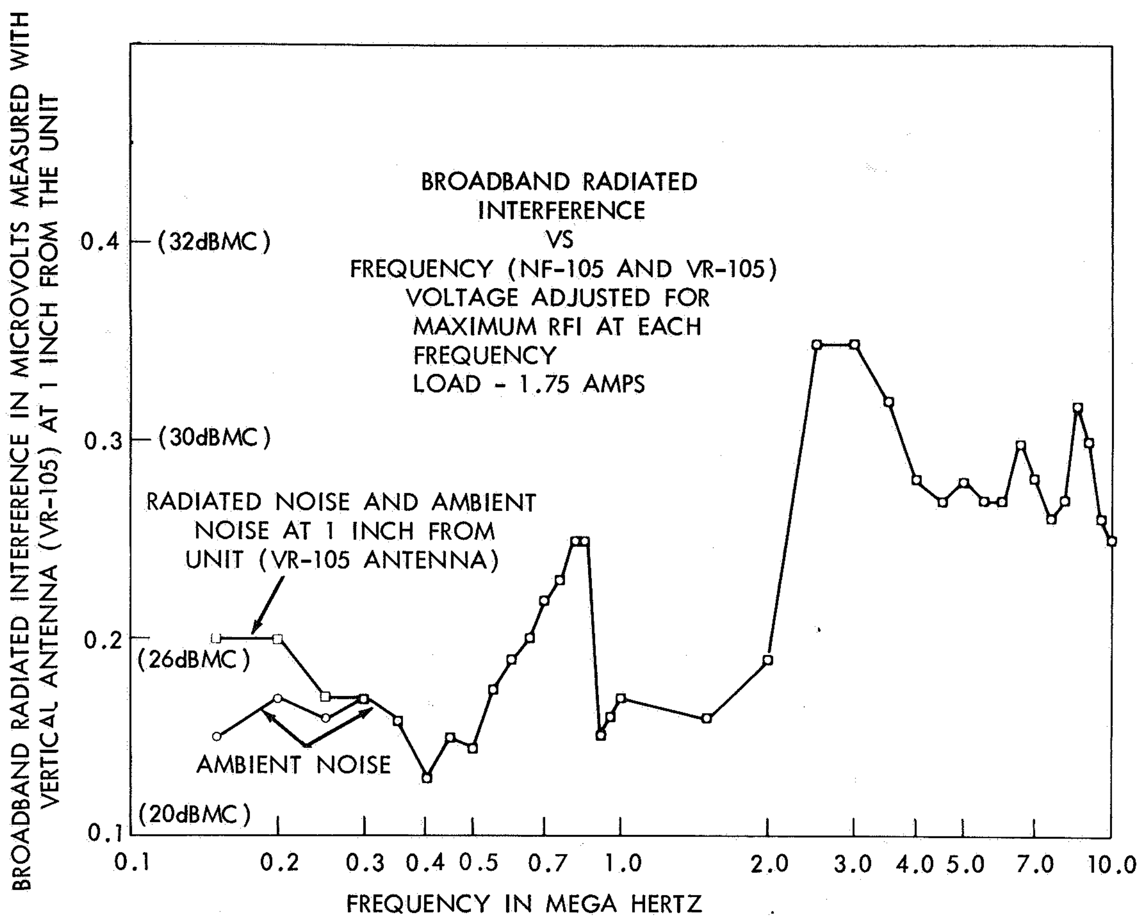


Figure 9b–Plots of Radiated RFI of RAE Pre-Regulator

transistors, and power diodes, were mounted on internal walls, while the smaller components comprising the control and sensing circuitry, etc., were mounted on printed circuit boards. The internal walls, in addition to serving as rigid mounting members, also provided the major heat flow path from the package to the vehicle structure.

To keep the resistance losses and the lead inductance to a minimum, all power wire runs were made as short as possible. In addition, the routing of leads in parallel or twisted pairs was also done where possible. A single point ground was established near the input connector to eliminate circulating ground currents and maintain control of the current flow in each ground lead.

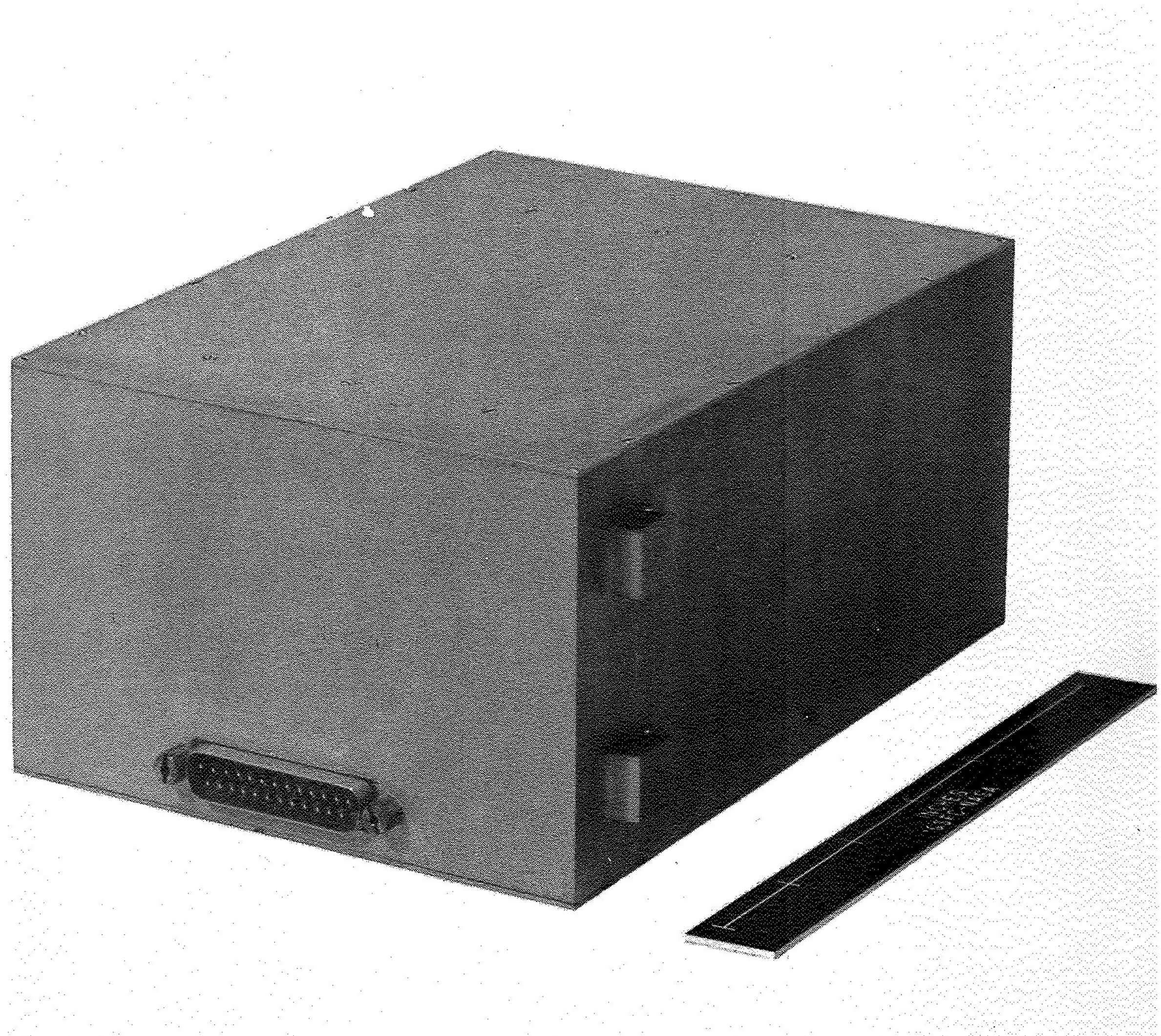


Figure 10a—Photograph of RAE Pre-Regulator with Cover Plates

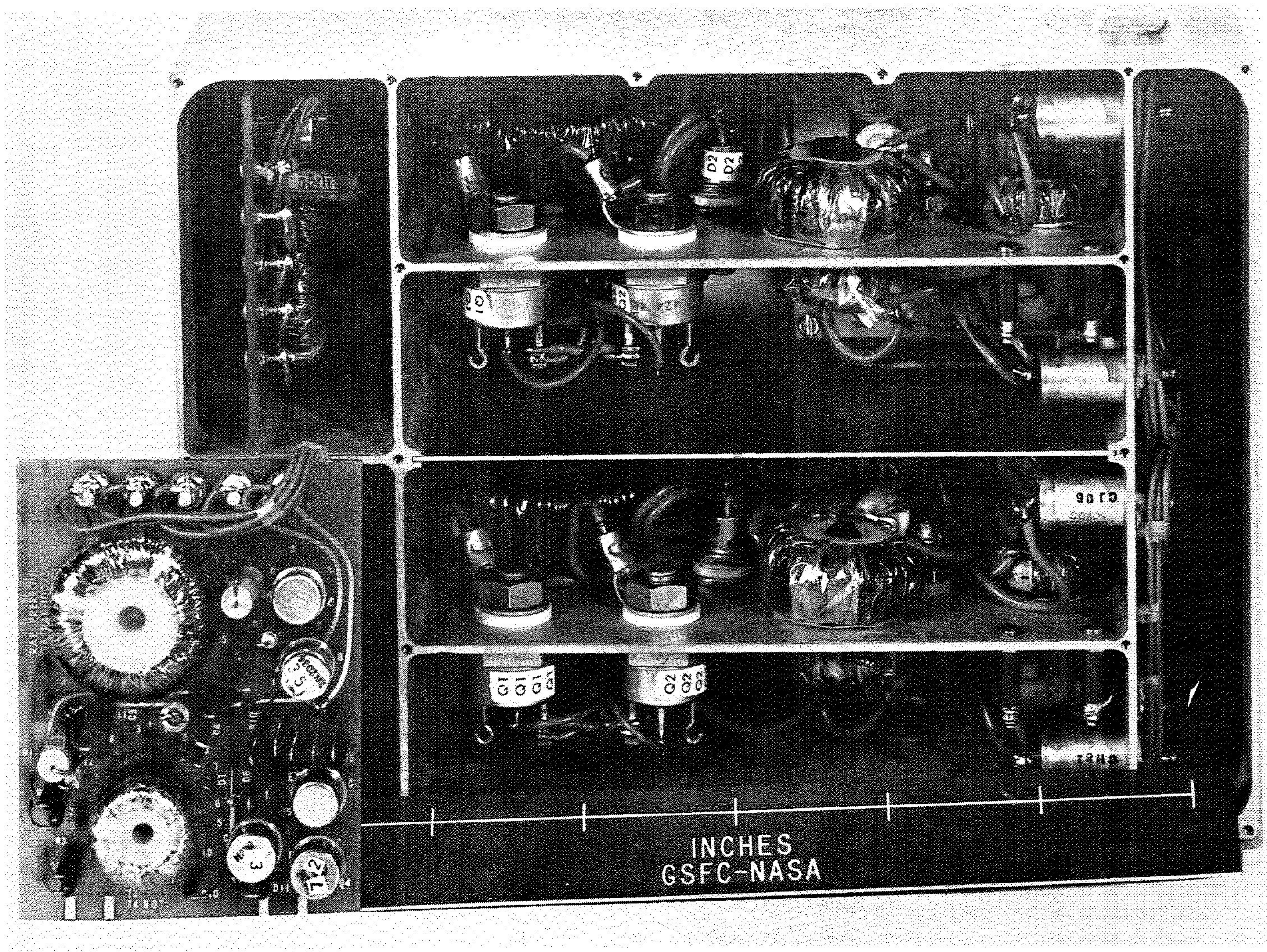


Figure 10b–Photograph of RAE Pre-Regulator with Top Cover Plate Removed and Plug in Printed Circuit Card Out

CONCLUSIONS

Power conversion and control is most efficiently accomplished with a considerable weight and volume savings by the use of a switching regulator. There are a number of different circuit techniques which can be used for control in such regulators, but regardless of the type chosen, the same basic RFI problem is present in varying degrees. The magnitude of the interference generated, however, is principally a function of the pulse energy transferred within the supply. This relates to the amplitude of the power switch currents and peak-to-peak ac voltage in the main power flow paths. When faced with the problem of minimizing RFI, quite often a necessity in the present space flight power supplies, the designer must carefully evaluate the basic regulation techniques in order to keep the RF filter and packaging requirements to a minimum. Significant gains in weight and performance can be realized when the RF problem is considered at the initial design phase. This report has demonstrated such an approach and its results.

The design and development of a main bus regulator with very low RFI for the RAE spacecraft has been presented. The selection of the regulation technique was based on minimization of the RFI, while maintaining the best overall performance. A variable-ratio dc boost transformer configuration, characterized by its minimum pulse energy transfer, was used after evaluation of a number of techniques. With this approach, a main bus regulator was designed which exhibited good static regulation, high efficiency, well defined output characteristics, good dynamic regulation and low RFI. The results indicate that very little sacrifice of performance was incurred by the use of this method, and the RFI was also kept at a minimum.

In the presentation of this technique, the equation giving the duty cycle of the power switches required to maintain a regulated output has been derived. In addition, the mathematical development of the critical inductance equation was presented.

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